UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/716,533 | 11/20/2003 | Hirotaka Tamura | 100021-00135 | 6886 |

4372 7590 12/05/2005

ARENT FOX PLLC
1050 CONNECTICUT AVENUE, N.W.
SUITE 400
WASHINGTON, DC 20036

| EXAMINER | |
|---|---|
| LAM, TUAN THIEU | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | |

DATE MAILED: 12/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/716,533 | TAMURA ET AL. | |
| | Examiner | Art Unit | |
| | Tuan T. Lam | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *3-12 and 14-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20 and 21* is/are allowed.

6)☒ Claim(s) *3,4,8,9 and 14-18* is/are rejected.

7)☒ Claim(s) *5-7,10-12, 19* is/are objected to.

8)☒ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This is a response to the amendment filed 10/20/2005. Claims 3-12 and 14-21 are pending and are under examination.

### *Claim Objections*

1. Claims 18-19 are objected to because of the following informalities: the recitation of "the input signals", "output signals" in lines 3 of claims 18 and 19 lacks proper antecedent basis.. Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 3-4, 8-9, 14-16 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Johnson (USP 6,081,162).

Figure 1 shows a buffer circuit device receiving differential input signals and outputting a differential output signals comprising a buffer circuit (108) receiving the input signals and outputting the output signals, a common mode level generator circuit (124) having a replica circuit (124) depending on a next stage (112A, 112B) and outputting a specific level of a common mode voltage for the output signals to be output from said buffer circuit, a common mode voltage detection circuit (128) detecting a common mode voltage of specific signals and a bias voltage adjusting circuit adjusting a bias voltage (127) to be supplied to said buffer circuit by comparing an output signal of said common mode level generator circuit with an output

signal of said common mode voltage detection circuit as called for in claims 4, 8-9, 14-15 and 18.

Regarding claim 3, the common mode voltage detection circuit (the output of 128 is equivalent to the common mode voltage of the buffer circuit 108).

Regarding claim 16, the common mode level generator circuit (124) inherently having a constant current source when one of a transistors within the generator circuit 124 is turned on.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3-4, 8-9 and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Volk (US 20030122593).

Figure 5 shows a buffer circuit device receiving differential input signals and outputting a differential output signals comprising a buffer circuit (P1, P2, N1, N2) receiving the input signals and outputting the output signals, a common mode level generator circuit (circuit not shown for generating the target Vcm of a next stage) and outputting a specific level of a common mode voltage for the output signals to be output from said buffer circuit, a common mode voltage detection circuit (R1 and C1) detecting a common mode voltage of specific signals and a bias voltage adjusting circuit adjusting a bias voltage (Iv) to be supplied to said buffer circuit by comparing an output signal of said common mode level generator circuit with an output signal of said common mode voltage detection circuit.

Volk reference does not disclose the common mode level generator circuit having a replica structure as that of the next stage as called for in claim 18. Figure 5 of Volk teaches that the target Vcm is the common mode voltage to be applied to the next stage. One skilled in the art would have recognized that having the common mode level generator circuit and the next stage circuit of similar structure would have a uniform common mode voltage thus minimizing discrepancy errors. Therefore, outside of non-obvious results, the obviousness of having both the common mode level generator circuit and the next stage circuit of similar structure will not be patentable under 35USC 103(a).

Regarding claim 3, figure 5 shows the common mode voltage detection circuit detects a common mode voltage of the output signals of said buffer circuit.

Regarding claim 16, the common mode level generator circuit inherently having a constant current source when one of a transistors within the generator circuit is turned on.

Regarding claims 4, 8-9, 14-15 and 17, figure 5 shows the limitations recited therein.

***Allowable Subject Matter***

6. Claims 5-7 and 10-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claim 19 is objected to but would be allowable if rewritten to overcome the objection noted above.

8. Claims 20-21 are presently allowed.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P. CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan T Lam
Primary Examiner
Art Unit 2816

11/24/2005